

CLAIMS

What is Claimed is:

1. A method of equalizing digital data signals, comprising the steps of:
demodulating and decoding an input signal having input data to produce a data
5 output;
remodulating the data output to produce a pseudo-training sequence including an
idealized input signal; and
generating equalizer parameters from the pseudo-training sequence.

- 10 2. The method of claim 1, wherein the step of generating equalizer
parameters from the remodulated data output comprises the steps of:
buffering the input signal; and
comparing the buffered input signal to the pseudo-training sequence to produce
the equalizer parameters.

- 15 3. The method of claim 2, wherein the step of demodulating and decoding an
input signal having input data to produce a data output comprises the steps of:
recovering the carrier and timing of the input signal to produce a carrier and
timing recovered signal;
20 demodulating the carrier and timing recovered signal to produce a demodulated
signal; and
decoding the demodulated signal to produce a received data signal.

- 25 4. The method of claim 3, wherein the step of remodulating the data output
to produce a pseudo-training sequence comprises the steps of:
re-encoding the received data signal to produce a re-encoded signal; and
remodulating the encoded signal to produce the training sequence.

5. The method of claim 4, wherein:

the step of decoding the demodulated signal to produce a received data signal comprises the steps of:

inner decoding the demodulated signal;

5 detecting synchronization bits in the inner decoded demodulated signal;

and

outer decoding the demodulated signal using the synchronization bits;

the step of re-encoding the received data signal to produce a re-encoded signal comprises the steps of:

10 outer encoding the received data signal to produce an outer encoded signal;

and

placing synchronization bits in the outer encoded signal;

inner encoding the outer encoded signal.

15 6. The method of claim 3, wherein:

the step of decoding the demodulated signal to produce a received data signal comprises the steps of:

inner decoding the demodulated signal;

detecting synchronization bits in the inner decoded demodulated signal;

20 and

outer decoding the demodulated signal using the synchronization bits;

the step of remodulating the data output to produce a pseudo-training sequence comprises the steps of:

inner encoding the inner decoded demodulated signal to produce a re-

25 encoded signal; and

remodulating the re-encoded signal.

7. The method of claim 1, wherein the input signal is equalized before being demodulated and decoded.

8. The method of claim 7, wherein the step of generating equalizer parameters from the remodulated data output comprises the steps of:
buffering the equalized input signal; and
comparing the buffered equalized input signal to the remodulated data output to
5 produce the equalizer parameters.

9. An apparatus for equalizing digital data signals, comprising:
means for demodulating and decoding an input signal having input data to produce a data output;
10 means for remodulating the data output to produce a pseudo-training sequence including an idealized input signal; and
means for generating equalizer parameters from the pseudo-training sequence.

10. The apparatus of claim 9, wherein the means for generating equalizer
15 parameters from the remodulated data output comprises:
means for buffering the input signal; and
means for comparing the buffered input signal to the pseudo-training sequence to produce the equalizer parameters.

20 11. The apparatus of claim 10, wherein the means for demodulating and decoding an input signal having input data to produce a data output comprises:
means for recovering the carrier and timing of the input signal to produce a carrier and timing recovered signal;
means for demodulating the carrier and timing recovered signal to produce a
25 demodulated signal; and
means for decoding the demodulated signal to produce a received data signal.

12. The apparatus of claim 11, wherein the means for remodulating the data output to produce a pseudo-training sequence comprises:

means for re-encoding the received data signal to produce a re-encoded signal; and
means for remodulating the encoded signal to produce the training sequence.

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13. The apparatus of claim 12, wherein:

the means for decoding the demodulated signal to produce a received data signal comprises:

means for inner decoding the demodulated signal;

10 means for detecting synchronization bits in the inner decoded demodulated signal; and

means for outer decoding the demodulated signal using the synchronization bits;

15 the means for re-encoding the received data signal to produce a re-encoded signal comprises:

means for outer encoding the received data signal to produce an outer encoded signal;

means for placing synchronization bits in the outer encoded signal; and
means for inner encoding the outer encoded signal.

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14. The apparatus of claim 11, wherein:
the means for decoding the demodulated signal to produce a received data signal
comprises:
means for inner decoding the demodulated signal;
5 means for detecting synchronization bits in the inner decoded demodulated
signal; and
means for outer decoding the demodulated signal using the
synchronization bits;
the means for remodulating the data output to produce a pseudo-training sequence
10 comprises:
means for inner encoding the inner decoded demodulated signal to produce
a re-encoded signal; and
means for remodulating the re-encoded signal.

15. 15. The apparatus of claim 9, wherein the input signal is equalized before
being demodulated and decoded.

16. The apparatus of claim 15, wherein the means for generating equalizer
parameters from the remodulated data output comprises:
20 means for buffering the equalized input signal; and
means for comparing the buffered equalized input signal to the remodulated data
output to produce the equalizer parameters.

17. An apparatus for equalizing digital data signals, comprising:
25 a demodulator for demodulating an input signal to produce a data output;
a modulator, communicatively coupled to the demodulator, for remodulating the data
output to produce a pseudo-training sequence including an idealized input signal; and
a parameter generation module, communicatively coupled to the modulator for
generating equalizer parameters from the pseudo-training sequence.

18. The apparatus of claim 17, wherein the input signal is coded, and the apparatus further comprises:

a decoder, coupled between the demodulator and the modulator, for decoding the demodulated input signal to produce the data output; and

5 a coder, coupled between the modulator and the processor, for encoding the remodulated data output to produce the pseudo-training sequence.

19. The apparatus of claim 17, further comprising:

an equalizer, communicatively coupled to the input signal, the demodulator, and
10 the parameter generation module; and
a buffer, coupled between the input signal and the parameter generation module, for buffering the input signal.

20. The apparatus of claim 19, wherein the parameter generation module
15 compares the buffered input signal to the pseudo-training sequence to produce the equalizer parameters.

21. The apparatus of claim 17, further comprising:

an equalizer, communicatively coupled to the input signal; and
20 a buffer, communicatively coupled between the equalizer and the processor, for buffering the equalized input signal.

22. The apparatus of claim 21, wherein the processor compares the buffered input signal to the pseudo-training sequence to produce the equalizer parameters.

23. The apparatus of claim 17, further comprising:
a timing recovery and carrier recovery module communicatively coupled between
the input signal and the demodulator;
an inner decoder communicatively coupled to the demodulator;
5 a synchronization bit detector, communicatively coupled to the decoder;
an outer decoder, communicatively coupled to the outer decoder, the outer decoder
producing a received data output based on the input signal;
an outer encoder, communicatively coupled to the outer decoder;
a synchronization module, communicatively coupled to the outer encoder, the
10 synchronization module for placing synchronization bits in the outer encoded signal;
an inner decoder, communicatively coupled to the synchronization module; and
an inner decoder communicatively coupled between the inner encoder and the
modulator.

15 24. The apparatus of claim 17, further comprising:
a timing recovery and carrier recovery module communicatively coupled between
the input signal and the demodulator;
an inner decoder communicatively coupled to the demodulator;
an synchronization bit detector, communicatively coupled to the decoder;
20 an outer decoder, communicatively coupled to the outer decoder, the outer decoder
producing a received data output based on the input signal; and
an inner decoder communicatively coupled between the inner decoder and the
modulator.